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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Rifaat, et al.
Serial No:	09/925,889
Confirmation No:	6192
Filed:	August 6, 2001
For:	DESPREAD SIGNAL RECOVERY IN DIGITAL SIGNAL PROCESSORS
Examiner:	Kevin Burd
Art Unit:	2631

MAIL STOP AF
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF JOSE FRIDMAN
UNDER 37 C.F.R. §1.131

Sir:

I, Jose Fridman state and declare the following:

1. I am an inventor on the above-identified application.

2. Prior to June 1, 2001, Applicants herein had conceived and reduced to practice the invention of each of claims 1-30 (as originally filed and as amended to the present).

3. Attached hereto as Exhibit A is a true copy, with personal information of the inventors and confidentiality notices redacted, of an invention disclosure document which describes the subject matter of, and was used to prepare, the above-identified application. This document is signed by inventor Rasekh Rifaat and a witness and is dated September 26, 2000. As this document shows, the invention of the claims in the above application were reduced to practice prior to June 1, 2001. As stated in Exhibit A, "Using the accelerated instruction, up to sixteen 8-bit complex multiply-accumulates may be performed every cycle."

4. There was no significant development on the invention done after June 1, 2001. The register design and despread instruction and operation were reduced-to-practice and included in the design for the TigerSHARC Digital Signal Processor product before June 1, 2001.

I, the undersigned, declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this document and any patent which may issue from the above-identified patent application.

Date: 8/16/2006

Jose Fridman

A0312/7412

ANALOG DEVICES

RECEIVED SEP 27 2000

INVENTION DISCLOSURE

For Legal Department use only

Disclosure No. ADI746-HUS **Cost Center No.** 4523
Date Submitted: 9-27-2000 **Division:** DSP
Vice President: Bob Conrad

(Where Necessary, Use Reverse Side or Separate Sheet to Complete Answers)

1. Title of the Invention: Despread for CDMA implementation

[**Note:** The first-listed inventor will be considered the primary inventor and primary contact for patent matters.]

2. Full Name of Inventor No. 1. (including middle name or initial, "Jr.", etc.)
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Full Name of Inventor No. 3. (including middle name or initial, "Jr.", etc.)
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If more than three inventors, please use separate sheets.

The Invention

3. Brief description of problem solved by invention, and of the invention itself (big-picture overview of invention - may be illustrated by attaching block diagrams, flow charts, etc.):

Efficient implementation of the chip rate processing algorithms known as Rake Finger Despread functions. There are several aspects to the invention: parallel implementation of the algorithm (Rake Finger Despreader) and hardware implementation on the ADSP-TS00x DSP. The algorithmic aspect is a SIMD style implementation of a Rake Receiver Finger Despread.

4. Detailed description and sketches of invention are to be found on the attached sheets, identified below:

ADSP-TS001 Accelerator Architecture & Micro-Architecture Definition
Chip Rate Acceleration on the TigerSHARC DSP
Using TigerSHARC to Implement Despreading Presentation
TigerSharc supporting Rake Receiver Functions with Soft Acceleration
Proposed Instructions for TigerSHARC Rake Receiver Operation

5. List any formal drawings, schematics, manuals (by chapter and section), etc. which describe the invention and its operating environment.

Please see above listed documents

6. Into what product(s) will this invention go, or what product(s) will this invention be used to make, test, design, etc. (include future generations).

ADSP-TS00x Family of Digital Signal Processors

The Prior Art

7. Closest prior art practices known to the inventor(s), including products/activities of Analog.

None

8. List any tangible record of prior art/practices known to the inventor(s) e.g., products, patents, manufacturing processes, brochures, printed publications, seminar presentations, product demos, etc.

9. Brief description of the reasons that the invention is different from the prior art practices, and of the advantages resulting from those differences.

In Prior art practices, the rake receiver has always been performed using a specialized ASIC or FPGA. This invention allows the speedup of this function to a point where it can be controlled and used as a software module allowing greater flexibility than was previously possible.

Invention Process and Documentation

10. The invention was first thought of on (date) 7/23/98, as evidenced by (notebook entry, etc.) Attached email from Jose Fridman to Jeff Stevens, Zvi Greenfield, and Andrew McCann.

11. The first written description of the invention occurred on (date)7/23/98, a copy of which is attached in the email listed in #10.

12. The first drawing or sketch occurred on (date) 8/9/00, a copy of which is attached in the ADSP-TS001 Accelerator Architecture & Micro-Architecture Definition.

13. The first disclosure of the invention to others within Analog, occurred on (date) 7/23/98, as evidenced by attached email listed in #10.

14. The invention was first shown to be operable in its intended environment on (date) 8/28/00
by: Rasekh Rifaat
(computer simulation, working prototype, process implementation, etc.) as evidenced
by: Computer Simulation

[Answer questions 15 and 16 if applicable. If inapplicable, write "N/A" in the appropriate blanks.]

15. The first disclosure of the invention to anyone outside of Analog (if any) occurred on (date) 8/16/2000
to Alcatel in Stuttgart, Germany pursuant to [NDA] agreement, dated on file.

16. The invention was first sold, sampled, offered for sale, or used to produce a product that ultimately was sold, on
(date) N/A as evidenced by: N/A

17. Signature(s) of inventor(s)

(1) Rasekh Rifaat Date 9/27/00

(2) ______________________ Date ________

(3) ______________________ Date ________

18. Signature(s) of witness(es)

(1) ______________________ Date 9/27/2000

(2) ______________________ Date ________

(3) ______________________ Date ________

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Chip Rate Acceleration on the TigerSHARC DSP

The TigerSHARC Digital Signal Processor is a balance of many parallel resources and high bus bandwidth. The parallel resources offer high computation rates at moderate clock speeds. The high bus bandwidth enables high data rate processing. The TigerSHARC DSP architecture is an excellent candidate for applications requiring extremely high throughput, such as the chip rate decoding algorithms for wireless communications. Chip rate algorithms such as the rake receivers operate on large blocks of data and require an extremely high amount of processing per output datum. These algorithms also contain parallel characteristics allowing the processing to be split across many resources. The TigerSHARC architecture is highly suited to the rake receiver function, and has instructions that specifically support key elements of the algorithms .

The following is a brief description of the TigerSHARC's specific support for chip rate processing (applicable to CDMA communication standards). The enhancements enable a few key features:

- single instruction for DESPREAD (bit complex multiply and accumulate)
- highly parallel implementation to allow up to 8 complex multiplies per cycle
- support for spreading factors from 4 to 256+
- support for Rake Receivers with a variable number of fingers.
- flexibility to add customer IP within the decoding algorithms

Receiver Chip Rate Processing

The core function of the receiver chip rate processor is to despread the incoming chip rate data, into output symbols at a lower data rate. The despread function is simply to multiply the scrambling code by the input data, and sum up over several data. In a Rake Receiver, this functionality is enhanced by performing this operation several times in parallel with several time delayed copies of the same signal, or signals from different attenas. Because of multipath effects, the Rake can combine several identical symbol streams which have slightly different paths into a stronger symbol stream.

The core operation for a despreader, is a complex multiply and accumulate engine. One of the inputs is the incoming data from the antennas (assumed to be 8 bit I and 8 bit Q). The other input is the complex scrambling code (1 bit I and 1 bit Q). These two values are multiplied and summed over the spreading factor. For example, if the spreading factor is 8, then 8 complex multiply and accumulates results in the output symbol.

The chip rate acceleration on the TigerSHARC is geared towards optimizing this core function to provide "soft" acceleration, i.e. a rake receiver finger becomes a piece of software. Using normal operation, two 16-bit complex multiply-accumulates may be performed every cycle. As well, the scrambling code must be expanded from a single bit to 16 bits and the input data must be expanded from 8 bits to 16 bits. Using the accelerated instruction, up to sixteen 8-bit complex multiply-accumulates may be performed every cycle. The overall performance improvement is a factor of 8 times better than by using the conventional multiply instruction. As well, the accelerated multiply accepts single bit inputs for the scrambling code saving time and memory space.

New Instruction Types

TRs += DESPREAD(Rmq, THRd) + TRn
Rs = TRs, TRs += DESPREAD(Rmq, THRd)
Rsd = DESPREAD(Rmq, THRd)

Function: Complex multiply of sample data in Rmq with scrambling code data in THRd. The result is optionally added to the previous result (TRn). If the result isn't added to the previous, then a new calculation is started, and the result is transferred to a normal compute block register for storing or further processing.

MIPS Estimates

The following table presents the TigerSHARC cycle requirements per chip rate input bit.

Spreading Factor	Inner Loop Cycles	Inner Loop Chips Processed	Estimated Cycles per Chip	Cycles to Process One UMTS Frame
[illegible]	13	128	0.1016	93600
8	11	128	0.0860	79200
16	10	128	0.0782	72000
32	19	256	0.0743	68400
64	37	512	0.0723	66600
128	73	1024	0.0713	65700
256	145	2048	0.0708	65250

Table 1. TigerSHARC Chip Rate Finger Performance. UMTS Frame is 921600 chips.

Using TigerSHARC to Implement Despreading.

ANALOG DEVICES

ADI DSP: The fastest Growing DSP Supplier

CDMA Systems

- A Narrowband signal is spread into a wideband signal.
- Despreading is the process of accumulating several spread chips into a signal.
- A complex-multiply accumulate is performed over the spreading factor.

Rake Receivers

- Because of multipath, several delays of the incoming chips is possible.
- By combining the effects of several paths, a better estimate may be made.
- A “Finger” is the term for the despread function of a given path.
- Several “fingers” together form a rake receiver.

Despread Function

- Input Parameters
  - Array of Chips, Number of Symbols
  - Spreading Factor
  - Scrambling Codes (OVSF, Cscramb)
  - Channel Estimates
  - Finger Delays
- Output: Array of Symbols.

SIMD Processing

- TigerSHARC has two compute units and parallel resources within each compute unit.
- In today's processor chip rate processing can be done as complex MACs.
- Waste of multiplier because there is only a multiply by +1 or –1.
- Code Examples.

TigerSHARC Improvements

- Increase the multiplier width x2
- Use the ALU to add/subtract (simulate a complex multiply).
- Create an accelerator block to perform the complex multiply.

Data Management

- Consider that two frames of data are stored continuously in memory from every antenna (up to ~12).
- Need to load 1 quad word to each block in each cycle.
- Every 8 cycles, need to read the scrambling code data.
- Every SF/2 cycles need to write the data.